IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: PARK, Ki Chon

Serial No.: 10/736,722

Title: Circuit and Method for Generating Internal Clock Signal

Filed: December 16, 2003

Group Art Unit: 2816

Examiner: Nguyen, Hai L.

Atty. Docket Number: 29936/39878

Customer No.: 04743

I hereby certify that this paper and the documents referred to as enclosed therewith are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on the date indicated: **November 7, 2005.**

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COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop Issue Fee
Commissioner for Patents
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Sir:

Applicant files this paper in response to the examiner's Statement of Reasons for Allowance provided with the Notice of Allowance mailed September 30, 2005. Applicant respectfully requests that the following comments be considered to clarify the examiner's general recitation of the elements of claims 1, 7, 14-16 and 18.

On pages 2 and 3 of the Reasons for Allowance, claims 1, 14-16 and 18 have been misquoted as reciting a "circuit for generating an internal clock signal (as shown in Fig. 3) and a method of use thereof". Each of claims 1 and 18 actually recites a circuit for generating an internal clock signal. Each of claims 14 and 16 actually recites a method of generating an internal clock signal. Claim 15 was previously cancelled. While the Reasons for Allowance may have meant to refer to claim 17 instead of claim 15, claim 17 actually recites a method of generating an internal clock signal. Accordingly, none of claims 14, 16 or 17 recites a "circuit for generating an internal clock signal", and none of claims 1 or 14-18 recites "a method of use thereof".

Regarding the examiner's general recitation of the elements, Applicant notes that while the examiner has essentially paraphrased elements of independent claims 1, 7, 16 and 18 as having specific structural limitations not disclosed or suggested in the prior art (with which the Applicant agrees), Applicant notes that the other independent claims, namely claims 14 and 17, do not recite the same language as in claims 1, 7, 16 and 18. In fact, claims 14 and 17 are method claims that do not include structural limitations, and Applicant submits that claims 14 and 17 are patentable as including limitations other than the limitations that the examiner has selected from claims 1, 7, 16 and 18. Further, while the examiner refers to Fig. 3, Fig. 3 is an example of a circuit for generating an internal clock signal and the claims are not limited thereto. In any event, Applicant submits that each of claims 1, 7, 14 and 16-18 should be interpreted to include and should be construed to be limited only to the specific elements actually recited therein. The claims should not, therefore, be limited in any manner based on the examiner's reference to Fig. 3 or the examiner's general recitation of elements of claims 1, 7, 16 and 18 within the examiner's Statement of Reasons for Allowance.

In addition to the reasons for allowance set forth in the allowance papers that were mailed in connection with the present application, it is respectfully submitted that the claims are allowable for the additional reasons that the invention defined by the language of the claims is neither anticipated by, nor would have been obvious when taken as a whole in view of, the art of record.

Respectfully submitted,

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